

What is claimed is:

- sub E17*
1. A multi-layer electrode for an integrated circuit, comprising:
- a conductive barrier layer;
 - 5 a first conductive liner deposited over the conductive barrier layer;
 - a second conductive liner deposited over the first conductive liner; and
 - a conductive layer deposited over the second
- 10 conductive liner, wherein the conductive layer and the first conductive liner comprise the same material.
- sub F1*
2. The multi-layer electrode according to Claim 1 wherein the second conductive liner comprises a
- 15 conductive oxide.
3. The multi-layer electrode according to Claim 2 wherein the second conductive liner is 20-50 Angstroms thick.
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- sub F1*
4. The multi-layer electrode according to Claim 3 wherein the conductive layer and the first conductive liner comprise Pt.
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5. The multi-layer electrode according to Claim 4 wherein the first conductive liner is 200-500 Angstroms thick.
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6. The multi-layer electrode according to Claim 5 wherein the conductive barrier layer comprises TaSiN.
7. The multi-layer electrode according to Claim 6 wherein the integrated circuit comprises a DRAM or an
- 35 FRAM.

8. A multi-layer electrode for an integrated circuit,
comprising:

a conductive barrier layer;

a first conductive liner deposited over the

5 conductive barrier layer;

a second conductive liner deposited over the first
conductive liner, the second conductive liner comprising
a conductive oxide; and

a conductive layer deposited on the second
10 conductive liner.

9. The multi-layer electrode according to Claim 8
wherein the second conductive liner is 20-50 Angstroms
thick.

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10. The multi-layer electrode according to Claim 8
wherein the conductive layer and the first conductive
liner comprise Pt.

20 11. The multi-layer electrode according to Claim 8
wherein the first conductive liner is 200-500 Angstroms
thick.

12. The multi-layer electrode according to Claim 8
25 wherein the conductive barrier layer comprises TaSiN.

13. The multi-layer electrode according to Claim 8
wherein the integrated circuit comprises a DRAM or an
FRAM.

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14. A method of fabricating an electrode of an integrated circuit, comprising:
- depositing a conductive barrier layer over a substrate;
 - 5 depositing a first conductive liner over the conductive barrier layer;
 - depositing a second conductive liner over the first conductive liner; and
 - 10 depositing a conductive layer over the second conductive liner, wherein the conductive layer and the first conductive liner comprise the same material.
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15. The method according the Claim 14 wherein depositing a second conductive liner comprises depositing a
15 conductive oxide.
16. The method according to Claim 15 wherein depositing the second conductive liner comprises depositing 20-50
20 Angstroms of the conductive oxide.
17. The method according to Claim 16 wherein depositing a conductive layer and depositing a first conductive liner comprise depositing Pt.
- 25 18. The method according to Claim 17 wherein depositing the first conductive liner comprises depositing 200-500 Angstroms of Pt.
19. The method according to Claim 18 wherein depositing
30 a conductive barrier layer comprises depositing TaSiN.
20. The method according to Claim 19 wherein the integrated circuit comprises a DRAM or an FRAM.

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